REMARKS

Claims 1-9 are pending in the application.

Claims 1-9 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Applicants' Admitted Prior Art ("AAPA") in view of U.S. Patent No. 6,662,216 to Lin. Applicants respectfully traverse the rejection.

Again, the Examiner asserted that AAPA discloses all aspects of the claimed invention except for the features of the claimed access controller of each processor. The Examiner relied upon Lin as a combining reference that allegedly teaches these features.

In response to Applicants' remarks in the previous Response to Office Action, the Examiner cited the description in col. 1, lines 34-36 of Lin of maintaining cache "coherency" as alleged suggestion of the features of the claimed "access controller...that does not have access privileged."

Applicants respectfully submit that the "coherency" described in Lin merely refers to the generic bus snooping described therein, where only write commands and memory addresses are "snooped" to determine whether data cached by a processor needs to be invalidated, whereupon the cache would be updated (and data "replaced") the next time the processor accesses the common memory. For instance, Applicants refer to col. 1 line 62 to col. 2, line 15 of Lin, which describes maintaining cache "coherency" as follows:

> "The caching devices (e.g. bus device 112) that are not involved in the write request monitor the write signal (not shown) on the command lines 102. When the write signal is asserted, the caching bus device 112 reads the address lines 104 and compares the address to the addresses of the information that the caching bus device 112 has cached. Upon a match, the caching bus device 112 ***invalidates*** the cached information, ***so the caching bus device 112 will have to read the new information from the slave bus device 110 when the caching bus device 112 next accesses the information***.
>
> Through the command lines 102 the bus system 100 transfers a "hold" signal (not shown) for preventing the master bus device 108 from performing the write command until after

> the other caching devices (caching bus device 112) have completed the write-signal-snooping and address-comparing functions. After the caching bus device 112 completes the snooping and comparing functions, the caching bus device 112 releases, or deasserts, the hold signal, so the master and slave bus devices 108 and 110 can continue with the write command." (Emphasis added)

Correspondingly, Lin describe, on col. 5, line 44 to col. 6, line 4,

> The bus snooping device 248 (FIGS. 4 and 6) (or the bus snooping logic 244, FIG. 5) uses conventional logic to monitor, or "snoop," the write signal transferred on the control lines 250 to detect when information is to be changed within any of the slave devices 214 and 216 (FIG. 4). The information, for which the primary storage is the slave devices 214 and 216, may also have been cached within the master device 208 (FIGS. 4 and 5) (or master device 212, FIGS. 4 and 6). Therefore, if the information is to be changed in the slave device 214 or 216, then the cached copy in the cache memory 242 (FIG. 5) (or cache memory 122, FIG. 6) will have to be invalidated (or replaced). To enable determining whether the information has been cached, the bus snooping device 248 also monitors the ***command lines 250 and the address lines 252***, so that, upon detecting the transfer of the write signal on the control lines 250, the bus snooping device 248 determines which slave device 214 or 216 is the receiving slave device 214 or 216 and the location therein where the information is to be written. The bus snooping device 248 then performs a conventional cache tag lookup procedure to determine whether the information has been cached. If so, then the bus snooping device 248 causes the information to be invalidated. While the bus snooping device 248 is performing the detection, lookup and invalidation procedures, it uses conventional logic to intercept, disable or delay the ready signal (not shown) on the control lines 250 with the information transfer enable signal 246 (FIG. 5 or 6) on the system bus 202, as described below." (Emphasis added)

Lin illustrates, in Fig. 7 thereof, command lines 250, address lines 252, and data lines 254. Thus, the "bus snooping" described in Lin, at most, suggests invalidating cached data by snooping only the command and address lines. And, in view of the above-cited description, Lin clearly only suggests cached data of a processor being "replaced" the next time the processor accesses the memory.

Again, Lin only includes a plain recognition that stale cached data needs to be replaced. And the cited portions of Lin only include description of "conventional logic" to monitor only "the write signal transferred on the control lines 250 to detect when information is to be changed within any of the slave devices 214 and 216 (Fig. 4)." Col. 5, lines 45-48 of Lin. If the data is cached, then the cache is "invalidated." Please see, e.g., col. 5, lines 65-66 of Lin.

Thus, even assuming, arguendo, that it would have been obvious to one skilled in the art at the time the claimed invention was made to combine AAPA and Lin, the combination would still have failed to disclose or suggest,

> "[a] multiprocessor system comprising a common memory and a number of processors connected via a common bus, only one processor being allowed to access same data area of said common memory at a time, wherein:
> said common memory is provided with a number of data areas that store data and with a control information area that stores control information indicating whether each of the data areas is in use;
> each processor is provided with a storage unit for storing same data and same control information as those stored in the common memory and with an access controller; and
> the access controller of a processor ***that does not have access privilege monitors data*** and addresses that flow on the common bus, ***accepts***, from the common bus, ***data*** written to said common memory and ***data*** read from said common memory ***and stores this data in a memory area, which is designated by said address, of the storage unit within its own processor***," as recited in claim 1. (Emphasis added)

Accordingly, Applicants respectfully submit that claim 1, together with claims 2-5 dependent therefrom, is patentable over the cited references for at least the foregoing reasons. Claims 6 and 9 incorporate features that correspond to those of claim 1 cited above, and are, therefore, together with claims 7-8 dependent from claim 6, patentable over the cited references for at least the same reasons.

In view of the remarks set forth above, this application is in condition for allowance which action is respectfully requested. However, if for any reason the Examiner should consider this application not to be in condition for allowance, the Examiner is respectfully requested to telephone the undersigned attorney at the number listed below prior to issuing a further Action.

Any fee due with this paper may be charged to Deposit Account No. 50-1290.

Respectfully submitted,

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